E246200
VLSI Circuits Design
(Digital Integrated Circuits)
Spring, 2019

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What is VLSI?

- VLSI stands for **V**ery **L**arge **S**cale **I**ntegration
- Integration of what? ⇒ Integration of circuits
- What are circuits? ⇒ Transistors and wires. Also, some *resistors*, *capacitors* and *inductors*.
- So, you know
  - Integrated circuits (ICs): many transistors / wires / passive components on one chip.
  - Very Large Scale Integration (VLSI): very many

Why Integrated Circuits?

- Small, fast, low energy consumption, and cheap!
  - Create components in parallel, cost no longer $\propto$ # of devices
- $$\text{Circuit Cost} = \frac{\text{Circuit Area}}{\text{Wafer Area}} \times \text{Fabrication Cost}$$
  - A device area = 10 μm $\times$ 10 μm
  - An 8-inch wafer area = $\pi \times$ (0.1 m $\times$ 0.1 m)
  - Process cost = NT$ 50000 (typically, $500 - $3000)

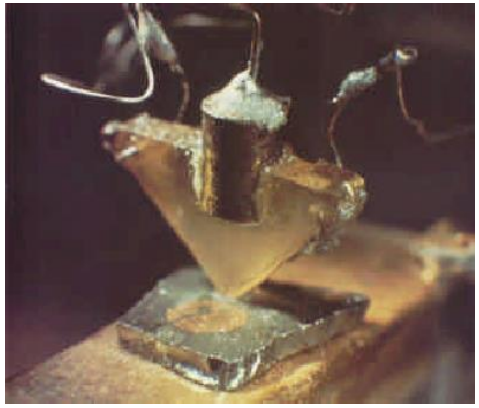
  $\Rightarrow$ Device cost NT$ 0.00016

  $\Rightarrow$ Cost of on-chip devices << Cost of off-chip devices
- For the same circuit
  - On-chip devices $\uparrow$ and off-chip devices $\downarrow$ $\Rightarrow$ Cost $\downarrow$

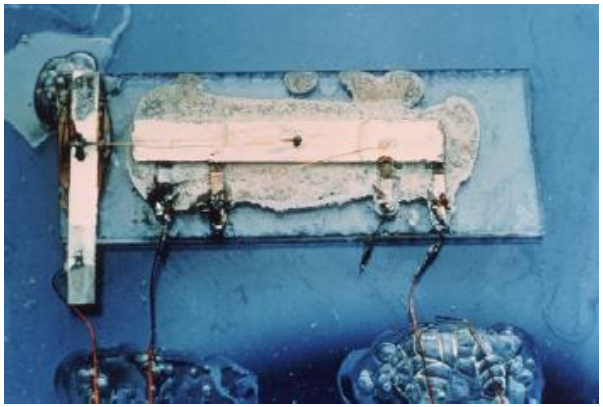
  $\Rightarrow$ High integration trend

A Brief History of ICs (1/2)

- Vacuum tubes ruled in first half of 20th century
  - Large, expensive, power-hungry, unreliable
- 1925: Field Effect Transistor theoretical development
  - by Julius Lilienfeld
- 1935: Modern FET structure
  - by Oskar Heil
  - Materials problems foiled early attempts to make functioning devices
- 1947: First point contact transistor
  - Invented by John Bardeen, Walter Brattain and William Shockley at Bell Labs (got Nobel prize)



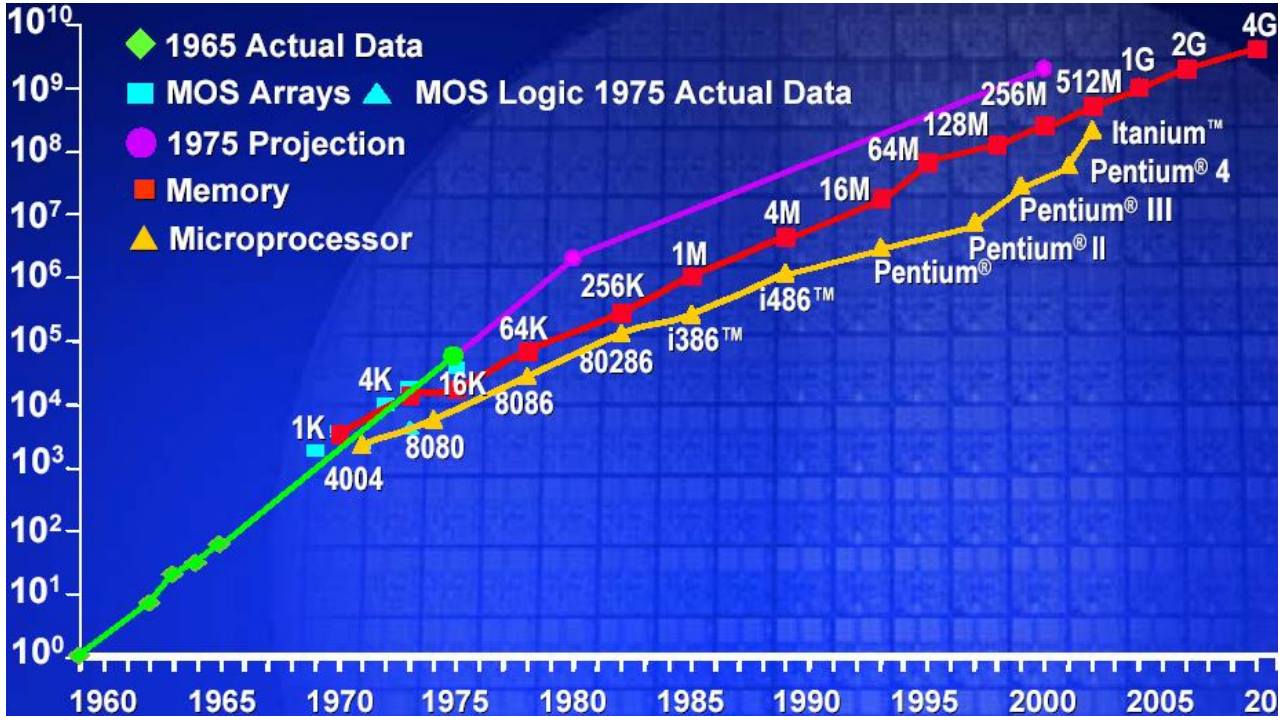
A Brief History of ICs (2/2)



- 1958: First integrated circuit
  - Flip-flop using two transistors
  - Built by Jack Kilby at Texas Instruments
- 2019
  - CPU: Graphcore GC2 IPU (16nm, 23.6 billion trs.)
  - GPU: Nvidia Volta V100 (12 nm, 21.1 billion trs., 5120 cores)
  - FPGA: Xilinx Versal/Everest (7 nm, 50 billion trs.)
- > 50% compound annual growth over 50 years
  - No other technology has grown so fast for so long

Moore's Law

- In 1965, Gordon Moore predicted that the number of transistors that can be integrated on a die would double every 18 months (i.e., grow exponentially with time).
  - Actually, double every 26 months (slow-down?)



Source: ISSCC 2003, G. Moore "No exponential is forever, but 'forever' can be delayed"

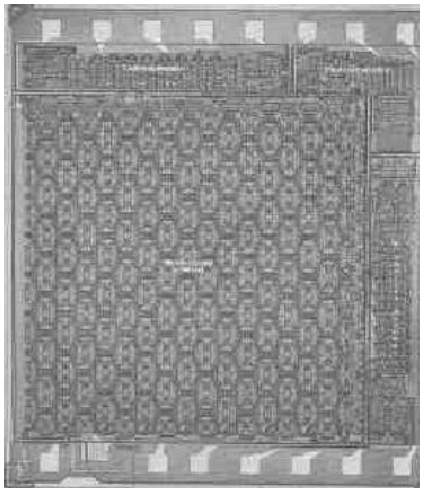
Transistor Types

- Bipolar transistors
  - *npn* or *pnp* silicon structure
  - *Small* current into very thin base layer controls *large* currents between emitter and collector
  - The quiescent power dissipated by the base currents limits integration density
- Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)
  - nMOS and pMOS
  - Voltage applied to insulated gate controls current between source and drain
  - Lower quiescent power consumption allows very high integration

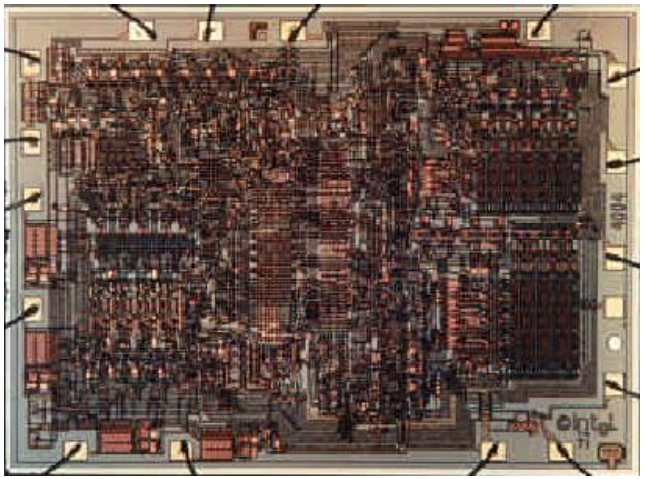
MOS Integrated Circuits

- 1960's processes used only pMOS transistors
  - Suffered from poor performance, yield, and reliability.
- 1970's processes usually had only nMOS transistors
  - Inexpensive, but consume power while idle

Intel 1101
256-bit SRAM

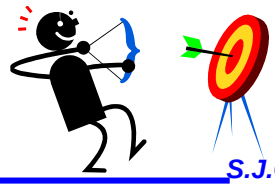


Intel 4004 4-bit
μ-Processor



- 1980s-present: CMOS processes were widely adopted for low idle power
  - CMOS stands for **C**omplementary **M**etal **O**xide **S**emiconductor.

Course Objective



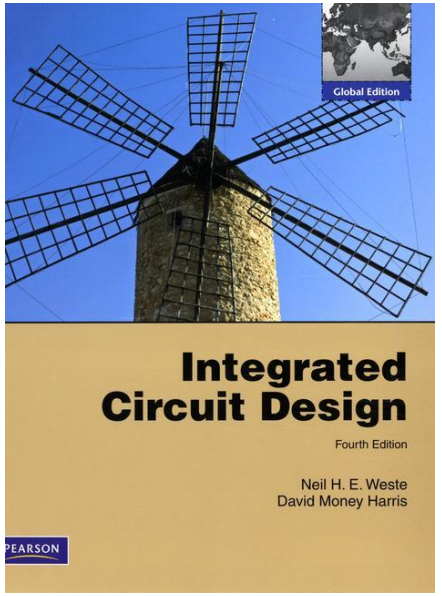
- To explore the design aspects involved in the realization of integrated circuits from device up to the system level
- It addresses major design methodologies with emphasis placed on structured full custom design
- It is expected to enhance the following knowledge/skills for the students
  - The models for state-of-the-art VLSI components, fabrication steps, layout technique, hierarchical design flow
  - Design and implement CMOS digital circuits and optimize them with respect to different constraints: size (cost), speed, power dissipation, and reliability
  - The VLSI CAD tool

Course Syllabus (1/2)

- Class Time: Wed. 9:10~12:00
- Classroom: Room 92225
- Instructor: 張順志
  - Email: soon@mail.ncku.edu.tw
  - Office: Room 95507 TEL: 06-2757575 ext. 62380
  - Office Hour: 14:00~17:00 on Wednesday and Thursday
- TA: 林柏翰、陳盈秀、邱薪育、何偉立、許哲維
  - Lab.: Room 95504
  - TEL: 06-2757575 ext. 62400 ext. 2810
- Prerequisites: An undergraduate-level course in electronic circuits and logic design.

Course Syllabus (2/2)

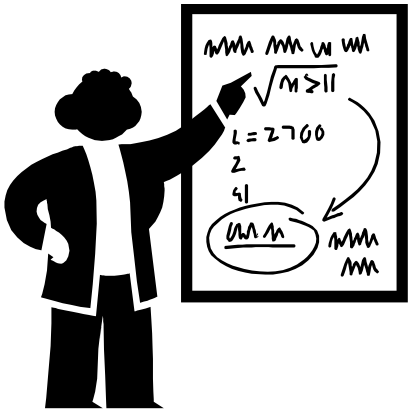
- Recommended Textbook
  - Neil H. E. Weste and David Money Harris, "Integrated Circuit Design: 4th Edition," Addison Wesley, 2010, ISBN: 0321547748



- Reference
  - R. Jacob Baker, "CMOS: Circuit Design, Layout, and Simulation, 3rd Edition," Wiley-IEEE, 2010, ISBN-13: 978-0470881323
  - Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective, 2nd edition", Prentice Hall, 2003, ISBN:0130909963

Course Contents

- Introduction
- CMOS fabrication
- CMOS layout
- Devices
- Speed
- Power
- Wires
- Gates
- Sequencing
- Datapaths
- Memories
- Packaging, Power, Clock, I/O



Schedule

Week	Date	Lecture	Note
1	2/20	Course overview	
2	2/27	Introduction to VLSI Design	
3	3/6	Fabrication	CAD tools training course; Homework #1 announced
4	3/13	Layout	
5	3/20	Devices	
6	3/27	Speed	Homework #1 due; Homework #2 announced
7	4/3		校際活動週(停課)
8	4/10	Power	
9	4/17	Wires	Homework #2 due; Homework #3 announced
10	4/24	Midterm Exam.	
11	5/1	Gates	
12	5/8	Scaling & Realiability	
13	5/15	Sequencing	Homework #3 due; Homework #4 announced
14	5/22	Datapaths	
15	5/29		停課一週
16	6/5	Memories	Homework #4 due; Homework #5 announced
17	6/12	Packaging, Power, Clock, I/O	
18	6/19	Final Exam.	9:10 ~ 11:00 exam.; Homework #5 due

Administrative Matters

- Grading Policy
  - Five Homeworks (50%)
  - Participation & Quiz (20%)
  - One Midterm Exam (15%)
    - April 24
  - One Final Exam (15%)
    - June 19
- Course Website
  - http://moodle.ncku.edu.tw/

This course has great materials, so HAVE FUN!